

What is claimed is:

- 1 1. An interconnect comprising:
2 a pad; and
3 at least two vias coupled to the pad.
- 1 2. The interconnect of claim 1, wherein at least one of the at least two vias is formed
2 substantially beneath the pad.
- 1 3. The interconnect of claim 2, wherein at least one of the at least two vias is
2 coupled to the pad by a conductive segment having a first end having a first width and a
3 second end having a second width, the first end being connected to the at least one of the
4 at least two vias and the second end being connected to the pad, and the first width being
5 less than the second width.
- 1 4. The interconnect of claim 2, wherein the pad has at least five substantially straight
2 edges and the at least two vias comprise three vias and only two of the three vias are
3 coupled to the substantially straight edges.
- 1 5. The interconnect of claim 4, wherein at least one of the only two of the three vias
2 coupled to the substantially straight edges is coupled to one of the substantially straight
3 edges through a tapered conductive segment.
- 1 6. A circuit substrate comprising:
2 a substrate;
3 a first pad formed on the substrate, the first pad coupled to a first potential plane;
4 a second pad formed on the substrate, the second pad coupled to a second
5 potential plane by at least three vias; and
6 a capacitor coupling the first pad to the second pad.

1 7. The circuit substrate of claim 6, wherein at least one of the at least three vias is
2 formed substantially beneath the second pad.

1 8. The circuit substrate of claim 6, wherein each of the at least three vias is formed
2 substantially beneath the second pad.

1 9. The circuit substrate of claim 8, wherein the capacitor comprises high frequency
2 capacitor.

1 10. The circuit substrate of claim 9, wherein the capacitor comprises a ceramic
2 capacitor.

1 11. A circuit substrate comprising:
2 a substrate;
3 a pad having a bottom surface, the pad formed on the substrate and the bottom
4 surface being in contact with the substrate; and
5 at least three vias coupled to the bottom surface.

1 12. The circuit substrate of claim 11, wherein the pad comprises a substantially square
2 core pad having four edges and three non-square pads, wherein each of the three non-
3 square pads is located adjacent to one of the four edges and is contiguous with one of the
4 four edges.

1 13. The circuit substrate of claim 12, wherein at least one of the three non-square pads
2 comprises a substantially triangular pad.

1 14. The circuit substrate of claim 13, wherein the substantially triangular pad is
2 coupled to one of the at least three vias.

1 15. The circuit substrate of claim 12, wherein each of the three non-square pads is
2 coupled to one of the at least three vias.

1 16. A method of forming an interconnect, the method comprising:
2 forming at least two vias in a substrate; and
3 coupling each of the at least two vias to a pad.

1 17. The method of claim 16, wherein coupling a pad to each of the at least two vias
2 comprises:
3 directly coupling the pad to at least one of the at least two vias.

1 18. The method of claim 17, further comprising:
2 forming a tapered conductive segment on the substrate to couple at least one of
3 the at least two vias to the pad.

1 19. The method of claim 18, further comprising:
2 electrically coupling an integrated circuit to the pad.

1 20. The method of claim 19, wherein electrically coupling an integrated circuit to the
2 pad comprises:
3 inserting a solder element between the integrated circuit and the pad.